deeper than 0.1 μm, and

wherein said first impurity region overlaps with each of said gate electrodes while each of said second impurity regions has an edge which coincides with that of each of said gate electrodes.

19 ~~44~~. (Amended) A semiconductor device according to claim 16 ~~41~~ wherein a floating gate is formed [on] over said first impurity region while said floating gate is not formed [on] over each of said second impurity regions.

REMARKS

Reconsideration and allowance of the subject application are respectfully requested.

The present invention is characterized by a flash memory.

Claims 21-44 are rejected under 35 U.S.C. 112, second paragraph.

Claims 27, 36, 40, and 44 are rejected under 35 U.S.C. 112 first and second paragraphs.

The foregoing claims have been amended to address these 112 rejections.

With respect to claim 33, applicants submit that this claim recites sufficiently the structure of the specific feature of this invention. That is, the relationship of the channel region to the first and second silicon films, and the

insulating film is clearly described.

It is thus urged the claims are now in accordance with 35 U.S.C. 112, first and second paragraphs.

Claims 21, 23, 28 and 30-32 are rejected under 35 U.S.C. 102 as unpatentable by U.S. Patent 5,254,865 to Koshimaru.

Claims 21-23 and 28-32 are rejected under 35 U.S.C. 102 as unpatentable by U.S. Patent 5,434,440 to Yoshitomi et al.

Claims 24-27 and 33-36 are rejected under 35 U.S.C. 103 as unpatentable over U.S. Patent 5,434,440 to Yoshitomi et al., and U.S. Patent 5,202,576 to Liu et al.

In the references cited in the Office Action, only Liu discloses a flash memory. Furthermore, applicants submit the present invention, as recited in the amended claims, differs from the references for the reasons given below.

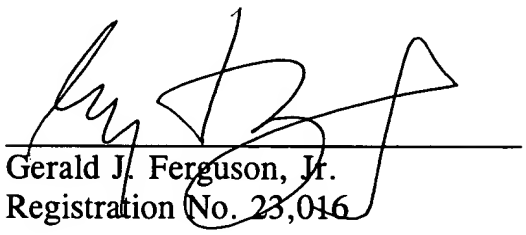
As shown in Fig. 2E of Liu, a shallower impurity region 22 overlaps with a gate electrode and a deeper impurity region 20 has an edge which is aligned with that of the gate electrode.

On the other hand, the amended claims recite that an edge of a shallower impurity region (a drain region) coincides with that of a gate electrode and a deeper impurity region (a source region) overlaps with the gate electrode, as shown in Fig. 9(E). Because the carrier is injected into the floating gate from the deep impurity region (page 19 lines 4-6), the deeper impurity region is the source region.

It is submitted the other references do not disclose the characterizing feature of the present invention as recited in the amended claims. Accordingly, applicants submit the differences between the references and the instant invention have been clarified.

In view of the foregoing amendments and remarks, it is urged this case is now in condition for allowance and a notice to that effect is requested.

Respectfully submitted,



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